(12) EUROPEAN PATENT APPLICATION

(54) Method of connection testing electronic boards.

(57) A method based on the observation that the clamping diodes (4, 8) between pins (2, 3) having similar functional characteristics form multicollector structures, which, when biased, supply comparable collector currents in the event of correct connection. The method therefore comprises stages consisting in grouping (30) the clamping diodes (4, 8) according to function or structure; biasing (32) the resulting multiterminal structures (10) so as to produce currents (I_{ci}); measuring (33) the currents; comparing (35, 36) the measured currents; and detecting (36, 37) faulty connections on the basis of marked variations in the currents.
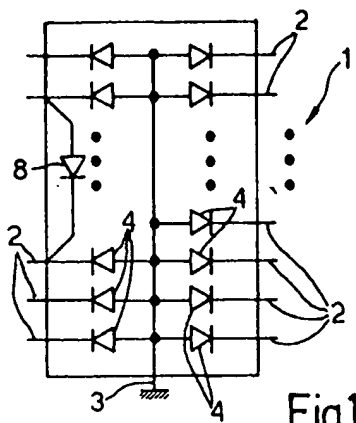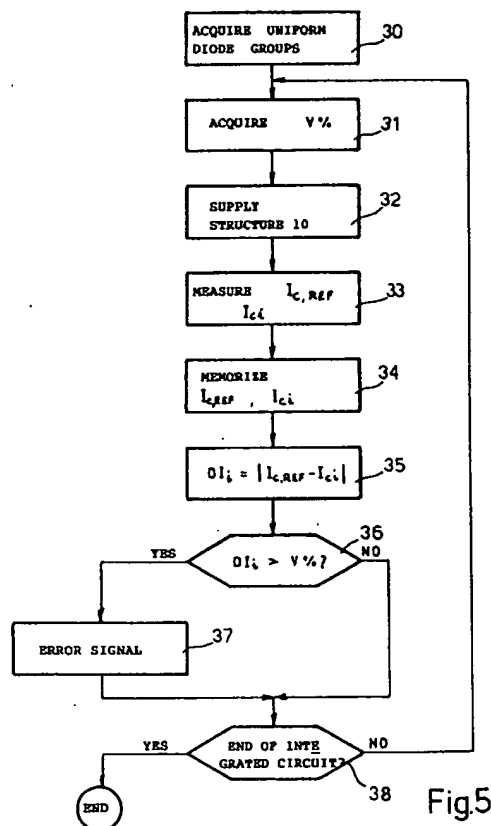
Fig.1

Fig.5

The present invention relates to a method of connection testing electronic boards.

For detecting errors made when assembling or soldering electronic components or integrated circuits to electronic boards, and which could jeopardize operation of the finished board, various test techniques are employed for detecting disconnected or short-circuited pins, inverted or missing components, or structural damage to the input/output stages.

Such techniques are divided into "hot" and "cold" systems. In the first, the board is supplied by an external circuit for generating appropriate test signals, after which, the system determines, via beds of needles or similar, that the electric quantities measured correspond with predetermined values within a given tolerance. Systems of this sort, however, are highly complex and expensive due to the external supply circuit. Cold test systems, on the other hand, provide for testing the board disconnected from the voltage supply, and in this sense are more straightforward and economical. One such system employed in the past uses clamping diodes between the ground pin and the other pins on each integrated circuit, as shown by way of example in Fig.1, which shows a schematic view of an integrated circuit 1 having a number of pins 2, one of which, indicated by 3, is grounded; clamping diodes 4 between pins 2 and pin 3; and a clamping diode 8 between two pins 2.

Clamping diodes 4 are formed as shown in Fig.2, which shows a cross section of the chip 5 of integrated circuit 1. Fig.2, in which the circuit 1 component layers and sinkers are omitted, shows a P type substrate 6, and the N type sinkers 7 connected to pins 2 and which, together with substrate 6, form PN junctions defining clamping diodes 4.

The above known system therefore consists in appropriately biasing the clamping diodes and measuring the current through them for detecting any disconnected or short-circuited components.

Though straightforward in both design and operation, the above system has not always been found to be entirely dependable and for this reason has by now been more or less abandoned. The characteristics of diodes 4, in fact, are not always known and, at any rate, are not consistent, by virtue of depending closely on the type of external connection of the pins (more specifically, on whether they are connected to external buses or other pins on another integrated circuit) and also on the type of signal for which the pin is designed. As a result, absolute measurement of the current through each pin cannot always be depended on for determining correct connection.

It is an object of the present invention to provide a connection test method of the second type,

i.e. of straightforward design and circuitry, which nevertheless provides for a high degree of reliability, even in the case of integrated circuits whose internal structure is unknown.

According to the present invention, there is provided a method of connection testing electronic boards comprising integrated circuits having pins and clamping diodes between said pins; characterized by the fact that it comprises stages consisting in:

identifying uniform groups of said diodes on the basis of functional or structural characteristics, for identifying multiterminal structures;

biasing said multiterminal structures so as to cause currents to flow through the terminals of said multiterminal structures;

measuring said currents at said terminals;

comparing said measured currents; and

detecting any faulty connections on the basis of marked variations in said currents.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Fig.1 shows an equivalent diagram of an integrated circuit with clamping diodes;

Fig.2 shows a cross section of a chip in which the clamping diodes are formed;

Fig.3 shows a circuit diagram of the equivalent multicollector structures formed by the clamping diodes of an integrated circuit:

Fig.4 shows a circuit diagram of a measuring system in accordance with the present invention;

Fig.5 shows a flow chart of the method according to the present invention.

The present invention is based on the fact that, on integrated circuits of the above type, various structures are obtainable by appropriately grouping the clamping diodes, that is:

a diode structure consisting of a diode between the ground pin and each other pin, or between two different pins;

a transistor structure consisting of two diodes between the ground pin and two different pins (the transistors in fact consist more or less of two antiseries PN junctions);

a multiemitter structure consisting of the diodes between the ground pin and the other pins, and which present similar functional and connection characteristics;

a multicollector structure, as above;

an SCR structure consisting of two series diodes, one between ground and a first pin, and the other between the first pin and a second pin (if any) on the integrated circuit.

Examination of the above structures has shown the transistor and SCR structures to be affected by

the same problems as the diode discussed earlier, whereas the multicollector or multiemitter structures can be used safely by virtue of the base-collector diodes (on the multicollector structure) being connected to pins having the same characteristics in terms of external connection and signal type. In fact, when current is injected between the base and a pin representing the emitter on the structure, the other pins function as collectors and, having the same functional and connection characteristics, tend to amplify the current accordingly. A marked difference in the collector currents thus indicates a faulty connection (short or disconnected circuits, wrong or ill-assembled components, damage to input/output stages).

Fig.3 shows an equivalent diagram of the clamping diodes in the Fig.1 circuit, grouped uniformly as described above according to the type of pin connection (bus or single component); the type of signals for which the pin is designed (e.g. analog, digital, address, data or control); and the level of the electric quantities involved. Each group thus defines a multicollector structure (Fig.3 shows three, 10a, 10b, 10c, respectively relative for example to bus-connected data, address and control signal pins) having its own base terminal 11 (grounded pin), its own emitter terminal 12 (one of the pins in the homogeneous group), and a number of collector terminals 13 (the other pins in the same group).

According to the present invention, each structure 10 is tested by biasing it, measuring the collector current at terminals 13, and checking that the difference in current (which is inevitable, due to production spread and an intrinsic amount of measuring inaccuracy) is below a given percentage of a given reference value.

For this purpose, each structure 10 is connected to a test apparatus 15 as shown in Fig.4. In the embodiment shown, apparatus 15 comprises a current source 16 connected between base terminal 11 and emitter terminal 12; a number of measuring branches 17 connected between emitter terminal 12 and respective collector terminals 13; and a processing logic circuit 18. More specifically, each measuring branch 17 comprises a series-connected voltage source 20 and ammeter 21; and logic circuit 18 comprises an interface 22 connected to ammeters 21 from which it receives the measuring result; a processing unit 23 connected to interface 22 and controlling the diagnostic stage; an input/output unit 24 connected to processing unit 23, for exchanging data, commands and information with the operator or an external system; and a data memory 25.

Fig.5 shows a flow chart of the various stages whereby each integrated circuit is tested according to the present system.

To begin with, block 30 provides for acquiring information relative to the diodes grouped uniformly as described above, i.e. connected to similarly connected pins designed for the same type of signal or electric quantity. This may be done by the operator entering the above data on input/output unit 24, or by reading memory 25, if the data has already been entered and stored for similar integrated circuits.

In the same way, block 31 then provides for acquiring the permitted percentage deviation of the collector currents in the diodes of the same group, which deviation is selected, for example, on the basis of the absolute value of the measured collector current and/or predictable spread according to the technology of the integrated circuit in question, as well as the type of pin connection and signal.

Block 32 then provides for enabling current source 16 and sources 20; and block 33 for acquiring, via interface 22, the I_{ci} current values measured by ammeters 21 and produced by amplifying the base current injected by source 16, and one of which constitutes reference value $I_{C,REF}$ with which the other collector currents are compared. The currents so detected are then memorized in block 34 and subsequently compared with one another. More specifically, for all the detected I_C values, block 35 provides for calculating the difference DI_i between the i-thy current I_{ci} and reference current $I_{C,REF}$, and block 36 for checking the differences are below the set deviation percentage V%. If they are not (collector currents below the minimum threshold or above the maximum threshold - YES output of block 36), an error signal is generated by block 37, possibly also indicating the faulty pin and the type of fault detected, after which, block 38 checks that all the homogeneous groups on the circuit have been tested. Block 38 is also reached in the event of the connections testing out correctly (NO output of block 36). When all the multicollector structures 10 on circuit 1 have been tested (YES output of block 38), the procedure is terminated (or repeated for other circuits on the same board). Conversely (NO output of block 38), block 38 goes back to block 31.

The advantages of the present invention will be clear from the foregoing description.

In particular, it provides for a straightforward, highly reliable method of connection testing integrated circuit pins, by virtue of the collector currents, in the event of correct connection, being comparable and varying within predetermined limits depending on the connection and operating characteristics of the pin, and regardless of the absolute value detected. Moreover, said absolute value need not necessarily be known beforehand, so that the test may also be applied to integrated circuits of unknown function, and of which are

known only the connections and the type and level of the electric quantities involved, as shown on any integrated circuit data sheet. In the case of integrated circuits of known type and known integrated components, the homogeneous diode groups constituting the multicollector structures may be acquired automatically; and the procedure described may be implemented in and form only part of a much wider test system.

Finally, the system according to the present invention is straightforward as regards both design and circuitry, and as such may be implemented easily and relatively cheaply.

To those skilled in the art it will be clear that changes may be made to the method as described and illustrated herein, in particular for adapting it to specific requirements, without, however, departing from the scope of the present invention. For example, instead of being measured simultaneously for all the collector-base diodes in the same group, collector currents I_{ci} may be measured sequentially, thus drastically simplifying apparatus 15 by reducing it to a single measuring branch 17, as well as interface unit 22 for acquiring the detected measurements.

The system may also provide for additional checks, e.g. for detecting faulty connection of the reference base-collector diode or base-emitter diode.

The collector currents may also be compared differently, by calculating a mean detected current value and comparing each collector current value with the mean value instead of a reference value. Also, the mean value or deviation may be calculated using various techniques as required.

Claims

1. A method of connection testing electronic boards comprising integrated circuits (1) having pins (2, 3) and clamping diodes (4, 8) between said pins; characterized by the fact that it comprises stages consisting in:
   identifying (30) uniform groups of said diodes (4, 8) on the basis of functional or structural characteristics, for identifying multiterminal structures (10);
   biasing (32) said multiterminal structures (10) so as to cause currents (I_{ci}) to flow through the terminals of said multiterminal structures;
   measuring (33) said currents at said terminals;
   comparing (35, 36) said measured currents; and
   detecting (36, 37) any faulty connections on the basis of a marked variation in said currents.

2. A method as claimed in Claim 1, characterized by the fact that said multiterminal structures consist of multicollector transistors (10).

3. A method as claimed in Claim 2, characterized by the fact that said biasing stage (32) comprises a stage consisting in supplying a bias current to a ground pin (3) of an integrated circuit (1), and applying a voltage difference between the emitter terminal and the other collector terminals of said multicollector structure (10).

4. A method as claimed in any one of the foregoing Claims from 1 to 3, characterized by the fact that said comparing stage (35, 36) comprises stages consisting in selecting a reference terminal, and comparing the current ($I_{C,REF}$) through said reference terminal with the currents (I_{ci}) at the other terminals.

5. A method as claimed in any one of the foregoing Claims from 1 to 3, characterized by the fact that said comparing stage (35, 36) comprises stages consisting in determining the mean value of the currents through said terminals, and comparing said measured currents with said mean value.

6. A method as claimed in any one of the foregoing Claims from 1 to 5, characterized by the fact that said measuring stage (33) is performed simultaneously for all said terminals.

7. A method as claimed in any one of the foregoing Claims from 1 to 5, characterized by the fact that said measuring stage (33) is performed sequentially, one terminal at a time.

8. A method as claimed in any one of the foregoing Claims from 1 to 6, characterized by the fact that said comparing stage comprises a stage consisting in calculating (35) the difference (DI_i) between a reference value ($I_{C,REF}$) and said measured values (I_{ci}); and by the fact that said faulty connection detecting stage comprises a stage consisting in determining (31) a permissible deviation (V%), comparing (36) said deviation with said difference, and generating (37) a faulty connection signal in the event said difference exceeds said deviation.

9. A method as claimed in any one of the foregoing Claims from 1 to 8, characterized by the fact that said uniform group identifying stage (30) consists in grouping the pins (2, 3) on said integrated circuit according to the type of con-

nection to other components and structures on
the board, the type of signals exchanged, and
the level of the electric quantities involved.

10. A system for connection testing electronic
boards comprising integrated circuits (1) with
pins (2, 3) and clamping diodes (4, 8) between
said pins; characterized by the fact that it
comprises means (30) for identifying uniform
groups of said diodes on the basis of func-
tional or structural characteristics, and so iden-
tifying multiterminal structures; means (16, 20)
for biasing said multiterminal structures (10) so
as to cause currents (I_{ci}) to flow through the
terminals (13) of said multiterminal structures;
means (21) for measuring said currents at said
terminals; means (36) for comparing said mea-
sured currents; and means for detecting faulty
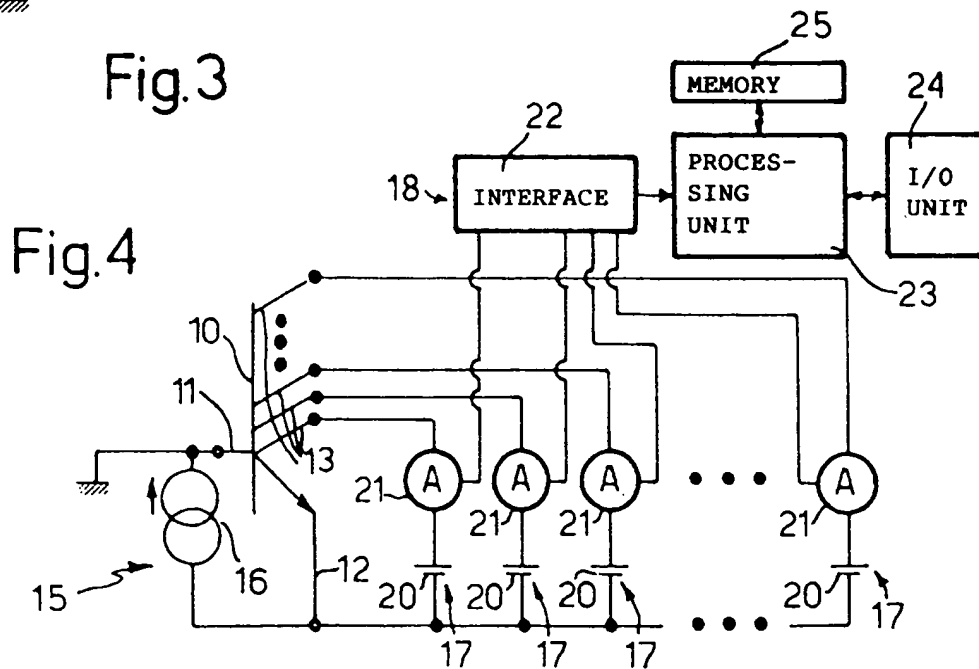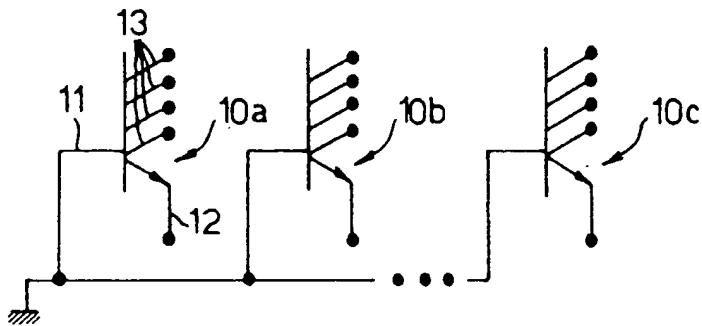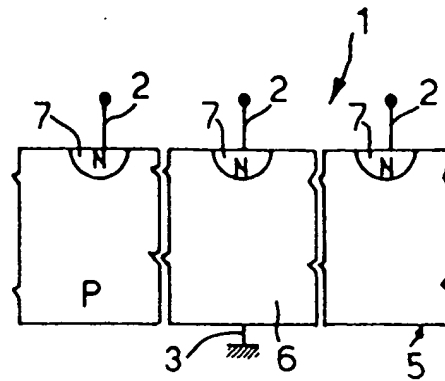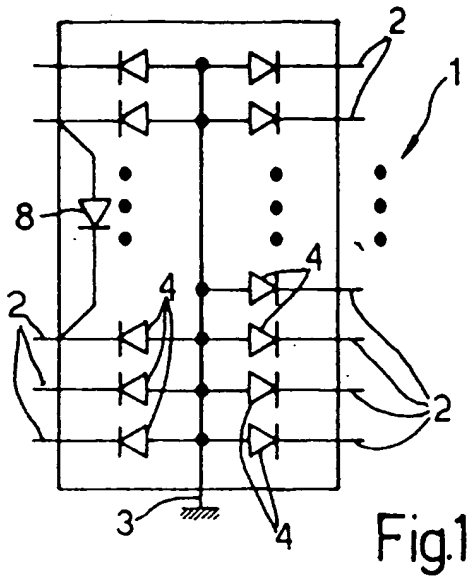connections on the basis of marked variations
in said currents.

Fig.1

Fig.2

Fig.3

Fig.4

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          ┌──────────────────┐
          │ ACQUIRE  UNIFORM │────30
          │ DIODE  GROUPS    │
          └──────────────────┘
                   │
                   ▼
          ┌──────────────────┐
          │ ACQUIRE    V %   │────31
          └──────────────────┘
                   │
                   ▼
          ┌──────────────────┐
          │ SUPPLY           │────32
          │ STRUCTURE 10     │
          └──────────────────┘
                   │
                   ▼
          ┌──────────────────┐
          │ MEASURE   I_c,REF│────33
          │         I_ci     │
          └──────────────────┘
                   │
                   ▼
          ┌──────────────────┐
          │ MEMORIZE         │────34
          │ I_c,REF , I_ci   │
          └──────────────────┘
                   │
                   ▼
      ┌──────────────────────┐
      │ DI_i = |I_c,REF - I_ci| │────35
      └──────────────────────┘
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$$DI_i = |I_{c,REF} - I_{ci}|$$

36

YES $DI_i > V\%$?   NO

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┌──────────────────┐
│  ERROR SIGNAL    │────37
└──────────────────┘
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YES   END OF INTE GRATED CIRCUIT?   NO

38

END

Fig.5